REMARKS

Reconsideration of the present application is respectfully requested.

The rejection of claim 1 under 35 USC 102(e) as being anticipated by Bowes et al. is respectfully traversed.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983); *SSIH Equip. S.A. v. USITC*, 718 F.2d 365, 218 USPQ 678 (Fed. Cir. 1983). Stated another way, for a prior art reference to anticipate in terms of 35 U.S.C. 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). (Emphasis added.)

Turning to the claim, claim 1 features:

(a) retrieving a first portion of the recorded data via the bus;

(b) updating some of the registers via the bus; ....

The Office Action implies that the bus of claim 1 corresponds to I/O bus 214 of Bowes et al. The Office Action further states that "therefore, updating the registers 314, 324 in the multiple DMA channels should be via the I/O bus 214." This perception of Bowes et al. is incorrect.

Looking at Fig. 2B, I/O bus 214 points to a junction that also is pointed to by leads to multiplexer 249 and 252. Multiplexers 249 and 252 are not registers. Also pointed to that junction is data bus 262. As shown in Fig. 3, data bus 262 is connected only to FIFO 310. Thus, Bowes et al. do not show any physical connection of I/O bus 214 to registers 314 and 324. This is clearly confirmed by the connections to registers 314 and 324 shown in Fig. 3. Thus, Bowes et al. do not identically show updating some of the registers via the bus as featured in claim 1. As such, claim 1 is not anticipated and is therefore allowable.

The rejection of claims 2-5 under 35 USC 103(a) as being unpatentable over Bowes et al. in view of Glover is respectfully traversed. Claims 2-5 depend from allowable claim 1. Bowes et al. are deficient in identically showing updating some of the registers via the bus as featured in claim 1. Glover does not overcome that deficiency. Therefore, claims 2-5 are not obvious and are allowable over these two applied references.

The rejection of claims 6, 8, 9, 11-14 under 35 USC 103(a) as being unpatentable over Bowes et al. and Glover and in view of Nishida is respectfully traversed.

Claim 6 features updating at least some of the read channel register values. The Office Action implies that references registers 314 and 324 are the read channel registers. This is incorrect. Registers 314 and 324 are used by the DMA channel depicted in Fig. 3. However, the DMA channel is not the same as a read channel. See Glover for further details. Then the registers 314 and 324 are not read channel registers. As a result, Bowes et al. do not identically shown read channel register values. Furthermore, the Office Action does not disclose where in the other applied references, Glover an Nishida, this claim 6 feature is identically shown. Therefore, claim 6 is not obvious over these three references and is allowable. In addition, claims 8, 9, 11-14 depend from claim 6. Since claim 6 is allowable, these claims are also allowable.

The rejection of claim 7 under 35 USC 103(a) as being unpatentable over Bowes et al., Glover and Nishida, and in further view of Asakawa et al. is respectfully traversed. As explained for claim 6, Bowes et al. are deficient in disclosing the feature of updating at least some of the read channel register values. None of the other three references used in this rejection have been cited to overcome this deficiency of Bowes et al. Therefore, claim 7 is allowable due to its dependence on allowable claim 6.

The rejection of claim 15 under 35 USC 103(a) as being unpatentable over Bowes et al. in further view of Nishida et al. is respectfully traversed. Claim 15 features a memory containing several values indexed by zone identifiers. The Office Action correctly points out that Bowes et al. do not identically show this feature. The Office Action relies on Nishida to show this feature by referring to Fig. 6B and col. 7, lines 30-

33. Figure 6B nowhere teaches or suggests a memory, so it cannot teach or suggest a memory containing several values indexed by zone identifiers. The reference to col. 7 is only the written description of Figure 6B. Again, there is no teaching or suggestion of a memory containing several values indexed by zone identifiers. Nor does the Office Action provide any objective evidence that would motivate or suggest to one skilled in the art such modification to either reference to arrive at that feature. Thus, claim 15 is not obvious over these references and is allowable.

As explained above, all the pending claims are patentable over the applied references. The examiner is respectfully requested to allow all the pending claims and pass this case to issuance.

Respectfully submitted,

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